

4x50G PD Array

PD4045-16M3-250T is a 4x50GBd Germanium photodetector array fabricated on silicon substrate, which is operating at wavelength range from 1260nm to 1360nm. 4 channels with 250μm pitch are integrated in one chip with 1130μm×360μm chip size. All G-S-G pads are on top side, the top-illumination make the device easy to assembly.

FEATURES

- 4-channel PD Array with 250μm Pitch
- Top-illuminated Device for Ease of Assembly
- G-S-G Pads on Top Side
- Operating at Wavelength Range from 1260nm to 1360nm
- AR Coating Optimized for Specified Wavelength
- Operating Temperature Range: -40 to 85°C

APPLICATIONS

- 400GBASE-DR4/FR4

KEY SPECIFICATIONS

Table 1. Key Specifications

Parameter	Symbol	Condition (T = 25°C, unless noted otherwise)	Rating			Unit
			Min.	Typ.	Max.	
Active Diameter	D	-	-	16	-	μm
Responsivity	R	$V_R = 3.0V, \lambda = 1310nm$	0.7	0.8	-	A/W
Dark Current	I_d	$V_R = 3.0V, 25^\circ C$	-	120	300	nA
		$V_R = 3.0V, 85^\circ C$	-	-	3000	
Breakdown Voltage	V_{br}	$I_d = 100\mu A$	10	-	-	V
Capacitance	C	$V_R = 3.0V, f = 1MHz$	-	80	100	fF
Linear Response saturation power	-	$V_R = 3.0V, \lambda = 1310nm$	10	-	-	dBm
3dB Bandwidth	BW	$V_R = 3.0V, R_L = 50\Omega$	26	28	-	GHz

ABSOLUTE MAXIMUM RATINGS

The table below provides maximum and/or minimum limits of critical parameters, limits listed in the table are stress limits only, and do not imply functional operation within these limits. Stresses beyond the limits may cause permanent damage. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Rating

Parameter	Symbol	Min	Max	Unit
Forward Bias Current	I_F	-	50	mA
Reverse Bias Voltage	V_R	-	10	V
Optical Input Power	P_{in}	-	10	dBm
Reverse Optical Current	I_R	-	10	mA
Storage Temperature	T_{stg}	-40	100	°C

RECOMMENDED OPERATING CONDITIONS

Table 3. Recommended Operating Conditions

Parameter	Symbol	Value	Unit
Operating Temperature	T_{op}	-40 ~ 85	°C
Operating Voltage	V_{op}	3	V
Wavelength Range	λ	1260 ~ 1340	nm
Baud Rate	B	53	GBaud
Optical Input Power	P_{IN}	-10 ~ 5	dBm

LAYOUT SCHEMATIC

- Both P (Anode) and N (Cathode) bonding pads on the top side
- Bonding pad size: $70\mu\text{m} \times 70\mu\text{m}$
- Die size: $1130 \pm 20\mu\text{m}$ (width) \times $360 \pm 20\mu\text{m}$ (length) \times $160 \pm 15\mu\text{m}$ (thickness)
- Channel pitch: $250\mu\text{m}$

Fig.1 Layout Schematic of PD4045-16M3-250T

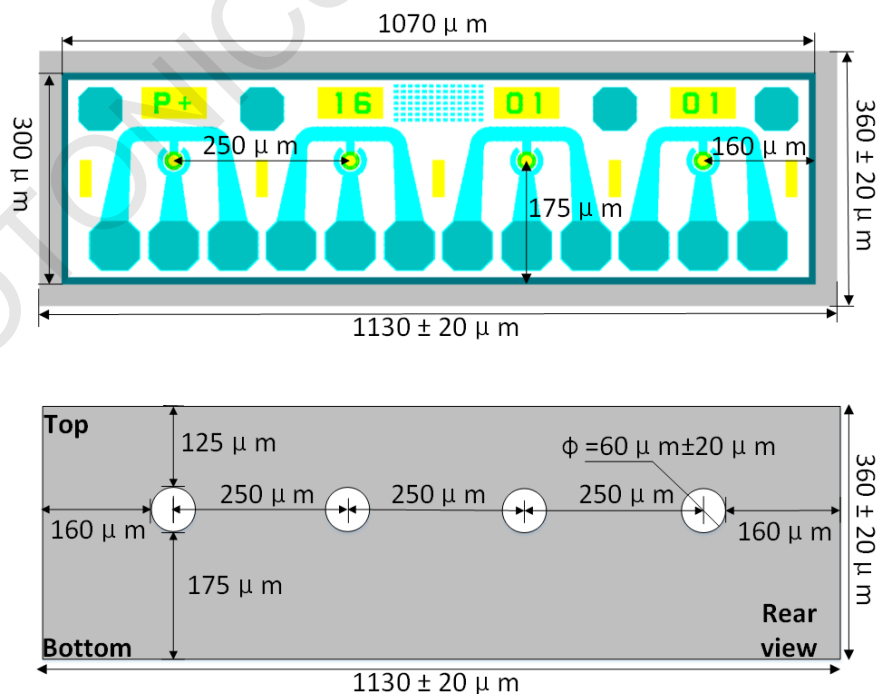
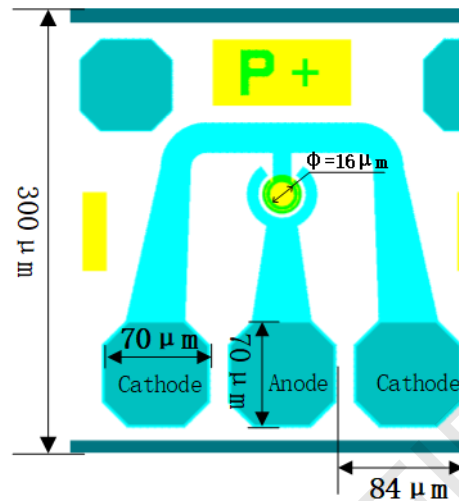


Fig.2 Aperture and Pad Layout Schematic


HANDLING PRECAUTIONS

1. This device is susceptible to damage as a result of electrostatic discharge, need take proper precautions during both handling and testing to avoid ESD damage and/or degradation.
2. Recommend to use a vacuum tip with a flat surface to handle this device, don't use tweezers to avoid any chip edge and/or pad broken.

REVISION HISTORY

Date	Revision	Changes
12/08/2021	1.0	Initial Version

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